# ADDITIONAL GATE CONTROL FOR A DOUBLE-GATE MOSFET

## TECHNICAL FIELD

**[0001]** The present invention relates to semiconductor devices and methods of manufacturing semiconductor devices. The present invention has particular applicability to double-gate devices.

## BACKGROUND ART

**[0002]** The escalating demands for high density and performance associated with ultra large scale integration semiconductor devices require design features, such as gate lengths, below 100 nanometers (nm), high reliability and increased manufacturing throughput. The reduction of design features below 100 nm challenges the limitations of conventional methodology.

**[0003]** For example, when the gate length of conventional planar metal oxide semiconductor field effect transistors (MOSFETs) is scaled below 100 nm, problems associated with short channel effects, such as excessive leakage between the source and drain, become increasingly difficult to overcome. In addition, mobility degradation and a number of process issues also make it difficult to scale conventional MOSFETs to include increasingly smaller device features. New device structures are therefore being explored to improve FET performance and allow further device scaling.

**[0004]** Double-gate MOSFETs represent new structures that have been considered as candidates for succeeding existing planar MOSFETs. In several respects, double-gate MOSFETs offer better characteristics than the conventional bulk silicon MOSFETs. These improvements arise because the double-gate MOSFET has a gate

electrode on both sides of the channel, rather than only on one side as in conventional MOSFETs. When there are two gates, the electric field generated by the drain is better screened from the source end of the channel. Also, two gates can control roughly twice as much current as a single gate, resulting in a stronger switching signal.

**[0005]** A FinFET is a recent double-gate structure that exhibits good short channel behavior. A FinFET includes a channel formed in a vertical fin. The FinFET structure may be fabricated using layout and process techniques similar to those used for conventional planar MOSFETs.

## SUMMARY OF THE INVENTION

**[0006]** Implementations consistent with the present invention provide a double-gate MOSFET that includes an additional gate control that provides increased design flexibility.

**[0007]** One aspect of the invention is directed to a method of manufacturing a semiconductor device. The method includes forming an insulating layer on a substrate, forming a fin structure on the insulating layer, the fin structure including a first side surface, a second side surface, and a top surface. The method further includes forming source and drain regions at ends of the fin structure and depositing a first gate material over the fin structure. The first gate material surrounding the top surface and the first and second side surfaces. Further, the method includes etching the first gate material to form a first gate electrode and a second gate electrode on opposite sides of the fin structure, planarizing the first gate material proximate to the fin structure, depositing a protective layer above the planarized first gate material and

the fin structure, and depositing second gate material on the protective layer and above the fin structure.

**[0008]** Another aspect consistent with the invention is directed to a device that includes a substrate, an insulating layer formed on the substrate, a conductive fin formed on the insulating layer, and gate dielectric layers formed on side surfaces of the conductive fin. The device further includes a first gate material layer formed on the insulating layer and around the conductive fin and a protective layer formed over the conductive fin and the first gate material. A second gate material layer is formed over the protective layer and the conductive fin.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0009]** Reference is made to the attached drawings, wherein elements having the same reference number designation may represent like elements throughout.

**[0010]** Fig. 1 is a diagram illustrating the cross-section of a semiconductor device;

**[0011]** Fig. 2A is a diagram illustrating the top view of a fin structure formed on the semiconductor device shown in Fig. 1;

**[0012]** Fig. 2B is a diagram illustrating a cross-section along line A-A' in Fig. 2A;

**[0013]** Fig. 3 is a diagram illustrating a cross-section of a gate dielectric layer and gate material formed over the fin structure shown in Fig. 2B;

**[0014]** Fig. 4 is a cross-section illustrating planarizing of the gate material shown in Fig. 3;

**[0015]** Fig. 5 is a diagram illustrating a top view of the device of Fig. 4;

**[0016]** Fig. 6 is a cross-section illustrating a protective layer formed over the device shown in Fig. 4;

**[0017]** Fig. 7 is a cross-section illustrating a gate material layer formed over the protective layer shown in Fig. 6;

**[0018]** Fig. 8 is a top view illustrating a semiconductor device shown in Fig. 7;

**[0019]** Fig. 9 is a cross-section illustrating planarizing of the gate material shown in Fig. 3 in an alternate implementation;

**[0020]** Fig. 10 is a diagram illustrating a top view of the device of Fig. 9; and

**[0021]** Fig. 11 is a cross-section illustrating the use of a T-shaped gate material layer.

## BEST MODE FOR CARRYING OUT THE INVENTION

**[0022]** The following detailed description of the invention refers to the accompanying drawings. The same reference numbers may be used in different drawings to identify the same or similar elements. Also, the following detailed description does not limit the invention. Instead, the scope of the invention is defined by the appended claims and equivalents.

**[0023]** A FinFET, as the term is used herein, refers to a type of MOSFET in which a conducting channel is formed in a vertical Si "fin." FinFETs are generally known in the art.

**[0024]** Fig. 1 illustrates the cross-section of a semiconductor device 100 formed in accordance with an embodiment of the present invention. Referring to Fig. 1, semiconductor device 100 may include a silicon on insulator (SOI) structure that includes a silicon substrate 110, a buried oxide layer 120 and a silicon layer 130 formed on the buried oxide layer 120. Buried oxide layer 120 and silicon layer 130 may be formed on substrate 110 in a conventional manner.

**[0025]** In an exemplary implementation, buried oxide layer 120 may include a silicon oxide and may have a thickness ranging from about 1000 Å to about 3000 Å. Silicon layer 130 may include monocrystalline or polycrystalline silicon and may have a thickness ranging from about 300 Å to about 1000 Å. Silicon layer 130 is used to form a fin structure for a double-gate transistor device, as described in more detail below.

**[0026]** In alternative implementations consistent with the present invention, substrate 110 and layer 130 may include other semiconducting materials, such as germanium, or combinations of semiconducting materials, such as silicon-germanium. Buried oxide layer 120 may also include other dielectric materials.

**[0027]** A dielectric layer 140, such as a silicon nitride layer or a silicon oxide layer (e.g., $SiO_2$), may be formed over silicon layer 130 to act as a protective cap during subsequent etching processes. In an exemplary implementation, dielectric layer 140 may be grown to a thickness ranging from about 150 Å to about 700 Å. Next, a photoresist material may be deposited and patterned to form a photoresist mask 150 for subsequent processing. The photoresist may be deposited and patterned in any conventional manner.

**[0028]** Semiconductor device 100 may then be etched and the photoresist mask 150 may be removed. In an exemplary implementation, silicon layer 130 may be etched in a conventional manner, with the etching terminating on buried oxide layer 120 to form a fin. After the formation of the fin, source and drain regions may be formed adjacent the respective ends of the fin. For example, in an exemplary embodiment, a layer of silicon, germanium or combination of silicon and germanium may be deposited, patterned and etched in a conventional manner to form source and

drain regions. In other implementations, silicon layer 130 may be patterned and etched to form source and drain regions simultaneously with the fin.

**[0029]** Fig. 2A schematically illustrates the top view of a fin structure 210 on semiconductor device 100 formed in such a manner. Source region 220 and drain region 230 may be formed adjacent the ends of fin structure 210 on buried oxide layer 120, according to an exemplary embodiment of the present invention.

**[0030]** Fig. 2B is a cross-section along line A-A' in Fig. 2A illustrating the formation of fin structure 210, which includes dielectric layer 140 and silicon layer 130 etched to the form shown in Figs. 2A and 2B.

**[0031]** Fig. 3 is a cross-section illustrating the formation of a gate dielectric layer and gate material over fin structure 210 in accordance with an exemplary embodiment of the present invention. A dielectric layer may be formed on silicon 130 of fin structure 210. For example, a thin oxide film 310 may be thermally grown on the fin portion of silicon layer 130, as illustrated in Fig. 3. The oxide film 310 may be grown to a thickness of about 10 Å to about 25 Å and may be formed on the exposed side surfaces of silicon layer 130. Alternatively, instead of a thin oxide film, a high-k gate dielectric such as $HfO_2$ may be deposited to a thickness of about 20 Å to about 40 Å.

**[0032]** A gate material layer 320 may be deposited over semiconductor device 100 after formation of the oxide film 310. In an exemplary implementation, gate material layer 320 may include polysilicon deposited using conventional chemical vapor deposition (CVD) or other well known techniques. Gate material 320 may be deposited to a thickness ranging from about 500 Å to 2800 Å. Alternatively, other semiconducting materials, such as germanium or combinations of silicon and germanium, or various metals may be used as the gate material. Gate material layer 320 forms a conductive gate for FinFET 100.

**[0033]** Fig. 4 is a cross-section illustrating the planarizing of the gate material 320 in accordance with an exemplary embodiment of the present invention. Excess gate material may be removed (e.g., from above dielectric layer 140) to planarize the fin region of the semiconductor device 100. For example, chemical-mechanical polishing (CMP) may be performed so that the gate material (i.e., layer 320) is even with or nearly even with dielectric cap 140 in the vertical direction, as illustrated in Fig. 4.

**[0034]** Referring to Fig. 4, the gate material layer 320 in the channel region of semiconductor device 100 abuts fin structure 210 on the two side surfaces to form a first gate 410 and a second gate 420. This structure is also shown in Fig. 5, which illustrates a top view of semiconductor device 100 consistent with the present invention. In Fig. 5, first gate 410 and second gate 420 are shown adjacent, but not covering, fin structure 210.

**[0035]** End portions of first gate 410 and second gate 420 may be patterned and etched to form two gate electrodes. As illustrated in Fig. 5, semiconductor device 100 includes a double gate structure with gate electrodes 510 and 520. Gate electrodes 510 and 520 are effectively separated by fin structure 210 and may be separately biased. For simplicity, the gate dielectric 310 (Fig. 4) surrounding the side surfaces of fin 210 is not shown in Fig. 5.

**[0036]** Referring to Fig. 6, a protective layer 610, such as an $SiO_2$ layer, may be formed over fin structure 210, first gate 410, and second gate 420. Protective layer 610 may be thermally grown to a thickness of about 150 Å to 300 Å.

**[0037]** Another gate material layer 720, shown in Fig. 7, may be deposited over protective layer 610. Gate material layer 720 may be patterned and etched to cover fin structure 210, as shown in Fig. 7. Gate material layer 720 may include polysilicon deposited using conventional CVD or other well known techniques. Gate material

720 may be deposited to a thickness ranging from about 200 Å to about 1000 Å. Alternatively, instead of polysilicon, other semiconducting materials, such as germanium or combinations of silicon and germanium, or various metals, may be used for gate material layer 720. Gate material layer 720 may be used as a third gate electrode for semiconductor device 100.

**[0038]** Fig. 8 is a top view illustrating semiconductor device 100 after etching gate material layer 720 to form a gate electrode, illustrated as gate electrode 830. Thus, at this point, semiconductor device 100 includes three gate electrodes: electrode 510, electrode 520, and electrode 830 that may each be separately biased. Alternatively, instead of placing gate electrode 830 directly above fin structure 210, gate material layer 720 may lead to one side of fin structure 210 in a manner similar to gate material 320 of gate electrodes 510 and 520. In this implementation, gate electrode 830 may be placed near one of gate electrodes 510 or 520.

**[0039]** The source/drain regions 220 and 230 may be doped. For example, n-type or p-type impurities may be implanted in source/drain regions 220 and 230. The particular implantation dosages and energies may be selected based on the particular end device requirements. One of ordinary skill in this art would be able to optimize the source/drain implantation process based on the circuit requirements and such acts are not disclosed herein in order not to unduly obscure the thrust of the present invention. In addition, sidewall spacers (not shown) may optionally be formed prior to the source/drain ion implantation to control the location of the source/drain junctions based on the particular circuit requirements. Activation annealing may then be performed to activate the source/drain regions 220 and 230.

**[0040]** In semiconductor device 100, as described above, gate material layer 320 was planarized such that fin structure 210 separated gate material layer 320 into first

and second separate gates 410 and 420, respectively. In alternate implementations, gate material layer 320 may be maintained as a single connected region. In this implementation, the final semiconductor device may only have two separately addressable gate electrodes.

**[0041]** Fig. 9 is a diagram illustrating a semiconductor device, labeled as semiconductor device 900, in which gate material layer 320 is maintained as a single connected region. Semiconductor device 900, as shown in Fig. 9, is similar to semiconductor device 100 as shown in Fig. 4, except in this implementation, the planarization process is stopped while gate material layer 320 is still over fin structure 210. Gate material layer 320 may then be patterned and etched to form a single gate electrode 1010 (Fig. 10). At this point, processing may proceed to add an additional gate electrode in the manner described about with reference to Figs. 6-8.

## OTHER IMPLEMENTATIONS

**[0042]** In order to act as an effective gate for semiconductor device 100, gate material layer 720 should be placed over fin structure 210. Accurately aligning gate material 720 over fin structure 210 to make an effective contact can, however, be difficult. To help alleviate this problem a T-shaped gate material layer may be used in place of gate material layer 720.

**[0043]** Fig. 11 is a cross-sectional diagram similar to Fig. 7, but illustrating the use of T-shaped gate material layer 1120 in place of gate material 720. In particular, as shown in Fig. 11, protective layer 610 is formed over fin structure 210 to include an indentation in the area over fin structure 210. When gate material layer 1120 is deposited, it fills in the indentation, thus potentially forming an effective contact with protective layer 610.

## CONCLUSION

**[0044]** A FinFET having three separately controllable gates is disclosed herein. The third gate may be biased independently of the other two gates and provides additional design flexibility in controlling the potential in the silicon fin during on/off switching.

**[0045]** In the previous descriptions, numerous specific details are set forth, such as specific materials, structures, chemicals, processes, etc., in order to provide a thorough understanding of the present invention. However, the present invention can be practiced without resorting to the specific details set forth herein. In other instances, well known processing structures have not been described in detail, in order not to unnecessarily obscure the thrust of the present invention.

**[0046]** The dielectric and conductive layers used in manufacturing a semiconductor device in accordance with the present invention can be deposited by conventional deposition techniques. For example, metallization techniques, such as various types of chemical vapor deposition (CVD) processes, including low pressure chemical vapor deposition (LPCVD) and enhanced chemical vapor deposition (ECVD) can be employed.

**[0047]** The present invention is applicable in the manufacturing of semiconductor devices and particularly in semiconductor devices with design features of 100 nm and below, resulting in increased transistor and circuit speeds and improved reliability. The present invention is applicable to the formation of any of various types of semiconductor devices, and hence, details have not been set forth in order to avoid obscuring the thrust of the present invention. In practicing the present invention,

conventional photolithographic and etching techniques are employed and, hence, the details of such techniques have not been set forth herein in detail.

**[0048]** Only the preferred embodiments of the invention and a few examples of its versatility are shown and described in the present disclosure. It is to be understood that the invention is capable of use in various other combinations and environments and is capable of modifications within the scope of the inventive concept as expressed herein.